DECLARATION

I, Shinichi Usui, a Japanese Patent Attorney registered No. 9694, of Okabe International Patent Office at No. 602, Fuji Bldg., 2-3, Marunouchi 3-chome, Chiyoda-ku, Tokyo, Japan, hereby declare that I have a thorough knowledge of Japanese and English languages, and that the attached pages contain a correct translation into English of the priority documents of Japanese Patent Application No. 10-65287 filed on March 7th, 1998 in the name of CANON KABUSHIKI KAISHA.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made, are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

signed this 7th day of November, 2002

SHINICHI USUI

PATENT OFFICE
JAPANESE GOVERNMENT

This is to certify that the annexed is a true copy of the following application as filed with this Office.

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Applicant(s): CANON KABUSHIKI KAISHA

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[Title of the Invention] SEMICONDUCTOR ELEMENT AND MANUFACTURING METHOD OF SEMICONDUCTOR ELEMENT

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[TITLE OF THE INVENTION] SEMICONDUCTOR ELEMENT AND MANUFACTURING METHOD OF SEMICONDUCTOR ELEMENT

[CLAIMS]

[CLAIM 1] A semiconductor element comprising microcrystalline semiconductor, having a semiconductor junction in a microcrystal grain.

[CLAIM 2] The semiconductor element according to claim 1 or 2, wherein the microcrystalline semiconductor comprises silicon atoms.

[CLAIM 3] The semiconductor element according to claim 1, wherein the microcrystalline semiconductor comprises germanium atoms.

[CLAIM 4] The semiconductor element according to any one of claims 1-3, wherein the microcrystalline semiconductor comprises hydrogen atoms.

[CLAIM 5] The semiconductor element according to any one of claims 1-4, wherein the microcrystalline semiconductor comprises halogen atoms.

[CLAIM 6] The semiconductor element according to any one of claims 1-5, wherein the microcrystal grain is columnar.

[CLAIM 7] A semiconductor element comprising a semiconductor layer having first electric characteristics, a semiconductor layer having second electric characteristics, and a semiconductor layer having third electric characteristics stacked in the named order, wherein a microcrystal grain is present extending over at least a portion of the semiconductor layer having the first electric characteristics and at least a portion of the semiconductor layer having the second electric characteristics.

[CLAIM 8] The semiconductor element according to claim 7, wherein a microcrystal grain is present extending over at least a portion of the semiconductor layer having the second electric characteristics and at least a portion of the semiconductor layer having the third electric characteristics.

[CLAIM 9] The semiconductor element according to claim 7 or 8, wherein one of the semiconductor layer having the first electric characteristics and the semiconductor layer having the third electric characteristics is a p-type semiconductor layer and the other thereof is an n-type semiconductor layer, and wherein the semiconductor layer having the second electric characteristics is an i-type semiconductor layer.

[CLAIM 10] A method of manufacturing a semiconductor element, comprising the steps of: forming a semiconductor layer having first electric characteristics on a substrate; crystallizing the semiconductor layer having the first electric characteristics; and growing a crystalline semiconductor layer having second electric characteristics on the crystallized semiconductor layer having the first electric characteristics, thereby growing a microcrystal grain so as to extend over the semiconductor layer having the first electric characteristics and the semiconductor layer having the second electric characteristics.

[CLAIM 11] A method of manufacturing a semiconductor element, comprising the steps of: forming a crystalline semiconductor layer having first electric characteristics on a substrate; and growing a crystalline semiconductor layer having second electric characteristics on the semiconductor layer having the first electric characteristics, thereby growing a microcrystal grain

so as to extend over the semiconductor layer having the first electric characteristics and the semiconductor layer having the second electric characteristics.

[CLAIM 12] A method of manufacturing a semiconductor element, comprising the steps of: forming a semiconductor layer having first electric characteristics on a substrate; growing a semiconductor layer having second electric characteristics on the semiconductor layer having the first electric characteristics; and effecting annealing to form a microcrystal grain so as to extend over the semiconductor layer having the first electric characteristics and the semiconductor layer having the second electric characteristics.

[CLAIM 13] A method of manufacturing a semiconductor element, comprising the steps of: forming a crystalline semiconductor layer on a substrate; and ion-implanting a dopant into the semiconductor layer to form a semiconductor junction in a microcrystal grain of the semiconductor layer.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[Field of the Invention]

The present invention relates to a semiconductor element and its manufacturing method, particularly to a functional semiconductor element such as a photovoltaic element and a thin film transistor and its manufacturing method.

[0002]

[prior Art]

Microcrystalline silicon semiconductors have been presented in 1979 (S. USUI and M. KIKUCHI, "PROPERTIES OF HEAVILY DOPED

GD-Si WITH LOW RESISTIVITY", Journal of Non-Crystalline Solids, 34 (1979), pp. 1 to 11). This article has described that a low-resistivity microcrystalline silicon semiconductor doped with phosphorous was able to be deposited by a glow discharge method.

[0003]

The same fact is described in A. MATSUDA, S. YAMASAKI et al., "Electrical and Structural Properties of Phosphorous-Doped Glow-Discharge Si:F:H and Si:H Films", Japanese Journal of Applied Physics, Vol. 19, No. 6, JUNE, 1980, pp. L305 to L308.

[0004]

Further, A. Matsuda, M. Matsumura et al., "Boron Doping of Hydrogenated Silicon Thin Films", Japanese Journal of Applied Physics, Vol. 20, No. 3, MARCH, 1981, pp. L183 to L186 discusses the characteristics of a mixed-phase of boron-doped amorphous and microcrystalline silicon.

[0005]

A. MATSUDA, T. YOSHIDA et al., "Structural Study on Amorphous-Microcrystalline Mixed-Phase Si:H Films", Japanese Journal of Applied Physics, Vol. 20, No. 6, JUNE, 1981, pp. L439 to L442 discusses the structure of an amorphous and microcrystalline mixed-phase.

[0006]

However, the possibility that such mixed layers of amorphous and microcrystalline silicon could be applied in semiconductor elements such as solar cells has been suggested, but there has been no actual application.

[0007]

Solar cells using microcrystalline silicon semiconductors have been described in U.S. Patent No. 4,600,801 "FLUORINATED P-DOPED MICROCRYSTALLINE SILICON SEMICONDUCTOR ALLOY MATERIAL", U.S. Patent No. 4,609,771 "TANDEM JUNCTION SOLAR CELL DEVICES INCORPORATING IMPROVED MICROCRYSTALLINE P-DOPED SEMICONDUCTOR ALLOY MATERIAL", and U.S. Patent No. 4,775,425 "P- AND N-TYPE MICROCRYSTALLINE SEMICONDUCTOR ALLOY MATERIAL INCLUDING BAND GAP WIDENING ELEMENTS, DEVICES UTILIZING SAME". However, the microcrystalline silicon semiconductors described in these patents have been used in p-type or n-type semiconductor layers in solar cells of a pin structure using an amorphous i-type semiconductor layer.

[0008]

Recently, articles on solar cells using microcrystalline silicon in an i-type semiconductor layer have been published. For example, there is "ON THE WAY TOWARDS HIGH EFFICIENCY THIN FILM SILICON SOLAR CELLS BY THE MICROMORPH CONCEPT", J. Meier, P. Torres et al., Mat. Res. Soc. Symp. Proc., Vol. 420, (1996) p. 3. However, as acknowledged by the authors of the article, the initial photoelectric conversion efficiency in a single structure solar cell using microcrystalline silicon in an i-type semiconductor layer is 7.7%, which is lower than that for solar cells with the same structure using amorphous silicon.

[0009]

[Problems to Be Solved by the Invention]

The present inventors have diligently inspected the reason why the conversion efficiency of solar cells using microcrystalline silicon semiconductors in an i-type semiconductor layer is lower

than that of amorphous silicon solar cells with the same structure. The results make clear that the main cause lies in the interfaces between the n-type semiconductor layer or the p-type semiconductor layer with the i-type semiconductor layer. Specifically, the present inventors have discovered that there are many defect states in the vicinity of the interface of the n-type semiconductor layer with the i-type semiconductor layer as well as in the vicinity of the interface of the p-type semiconductor layer with the i-type semiconductor layer, which function as recombination centers. The existence of the recombination centers results in reduction in number and lowering in transportability of photo-excited free carriers in the i-type semiconductor layer. As a result, the open circuit voltage (Voc), short-circuit current (Jsc), and fill factor (FF) of the solar cell decline. Further, it is attributable to an increase in series resistance and a decline in the shunt resistance of the solar cell . As a result, the conversion efficiency of the solar cell declines.

[0010]

When the inventors teamed up a transmission electron microscope with a secondary ion mass spectrometer and searched for the cause of the many defect states in the vicinity of the interfaces mentiond above, they discovered that the n-type semiconductor layer and the i-type semiconductor layer, or the p-type semiconductor layer and the i-type semiconductor layer were discontinuously stacked. Thus, they assumed that the reason why there were many defect states in the vicinity of the interfaces mentioned above was that the n-type semiconductor layer and the i-type semiconductor layer, or the p-type semiconductor layer

and the i-type semiconductor layer were discontinuously stacked.

[0011]

Further, when usual semiconductor elements are left to stand in the atmospheric environment, molecules in the air (water, oxygen, nitrogen, nitrogen oxides, sulfurous compounds, etc.) or the elements contained therein may sometimes diffuse into the semiconductor element to lower the characteristics of the semiconductor element. Similarly, when a semiconductor element such as a solar cell is encapsulated with another material (encapsulant), a chemical substance (acetic acid, etc.) contained in the encapsulant may sometimes diffuse into the semiconductor element to lower the characteristics of the semiconductor element. In particular, when each layer is stacked discontinuously at the semiconductor junction (junction of n-type semiconductor layer with i-type semiconductor layer, junction of p-type semiconductor layer with i-type semiconductor layer, etc.), the diffused substance will be trapped by the interface defects to lower the semiconductor characteristics.

[0012]

The present invention aims to solve the above-mentioned problems and improve the photoelectric conversion efficiency of a photoelectric conversion element represented by a solar cell.

[0013]

The present invention also aims to eradicate the discontinuity in the semiconductor junction portion to thereby provide a semiconductor element with superior semiconductor characteristics.

[0014]

In addition, the present invention aims to improve the heat resisting properties and durability of a semiconductor element.

[0015]

[Means for Solving the Problems]

A first aspect of the present invention is directed to a semiconductor element comprising microcrystalline semiconductor, having a semiconductor junction in a microcrystal grain.

[0016]

A second aspect of the present invention is directed to a semiconductor element comprising a semiconductor layer having first electric characteristics, a semiconductor layer having second electric characteristics, and a semiconductor layer having third electric characteristics stacked in the named order, wherein a microcrystal grain is present extending over at least a portion of the semiconductor layer having the first electric characteristics and at least a portion of the semiconductor layer having the second electric characteristics.

[0017]

A third aspect of the present invention is directed to a method of manufacturing a semiconductor element, comprising the steps of: forming a semiconductor layer having first electric characteristics on a substrate; crystallizing the semiconductor layer having the first electric characteristics; and growing a crystalline semiconductor layer having second electric characteristics on the crystallized semiconductor layer having the first electric characteristics, thereby growing a microcrystal grain so as to extend over the semiconductor layer having the

first electric characteristics and the semiconductor layer having the second electric characteristics.

[0018]

A fourth aspect of the present invention is directed to a method of manufacturing a semiconductor element, comprising the steps of: forming a crystalline semiconductor layer having first electric characteristics on a substrate; and growing a crystalline semiconductor layer having second electric characteristics on the semiconductor layer having the first electric characteristics, thereby growing a microcrystal grain so as to extend over the semiconductor layer having the first electric characteristics and the semiconductor layer having the second electric characteristics.

[0019]

A fifth aspect of the present invention is directed to a method of manufacturing a semiconductor element, comprising the steps of: forming a semiconductor layer having first electric characteristics on a substrate; growing a semiconductor layer having second electric characteristics on the semiconductor layer having the first electric characteristics; and effecting annealing to form a microcrystal grain so as to extend over the semiconductor layer having the first electric characteristics and the semiconductor layer having the second electric characteristics.

[0020]

A sixth aspect of the present invention is directed to a method of manufacturing a semiconductor element, comprising the steps of: forming a crystalline semiconductor layer on a substrate; and ion-implanting a dopant into the semiconductor layer to form

a semiconductor junction in a microcrystal grain of the semiconductor layer.

[0021]

[Embodiments]

The present inventors have performed a rigorous investigation in order to solve the above mentioned problems. As a result, it has been found that in a semiconductor element comprising microcrystalline semiconductor, an effective way to solve such problems is providing a semiconductor junction within a microcrystal grain. In the semiconductor element, at least a portion of each of two semiconductor layers with different electric characteristics (for example a portion of the n-type semiconductor layer and a portion of the i-type semiconductor layer or a portion of the p-type semiconductor layer and a portion of the i-type semiconductor layer) are formed in the vicinity of the interface between the layers within the same microcrystal grain. In other words, in the semiconductor element, there are microcrystal grains that extend over two semiconductor layers. In this way, by forming a semiconductor junction such as p/i or n/i within microcrystal grains, defect states in the vicinity of the interface can be reduced to a great extent. As a result, declines in the open circuit voltage (Voc), short circuit current (Jsc), and fill factor (FF) of a solar cell are prevented. Further, increase in the series resistance and decrease in the shunt resistance of a solar cell can be prevented. As a result, the conversion efficiency of the solar cell can be improved.

[0022]

Further, the heat resisting properties of the semiconductor

element can be improved by forming a semiconductor junction within microcrystal grains.

[0023]

In addition, discontinuity in layer interfaces in the semiconductor junction portion can be eliminated and the characteristics of the semiconductor element are improved by forming a semiconductor junction within the microcrystal grains. For example, by forming a semiconductor junction within the microcrystal grains, a depletion layer of a semiconductor junction expands further than in conventional semiconductor elements having a semiconductor junction. As a result, the rectifying characteristics are better than in a conventional semiconductor junction, and the dark current when applied with a reverse bias can also be kept low.

[0024]

A photovoltaic element is taken as an example of the semiconductor element of the present invention and is explained referring to the drawings hereinafter.

[0025]

Fig. 1 shows an example of the layer structure of a photovoltaic element, which is an example of the semiconductor element of the present invention. This photovoltaic element is composed of a substrate 111 (an electroconductive substrate comprised of a metal such as stainless steel or an insulating substrate comprised of glass or the like), with a reflection layer 110 comprised of a metal such as Al, Cu, or Ag, a reflection increasing layer 109 comprised of a metallic oxide or the like such as zinc oxide, indium oxide, or tin oxide, a bottom photovoltaic element

112 comprising an n-type or p-type semiconductor layer (the layer having the first electric characteristics) 108, an i-type semiconductor layer (the layer having the second electric characteristics) 107, and a p-type or n-type semiconductor layer (the layer having the third electric characteristics) 106 and a top photovoltaic element 113 comprising an n-type or p-type semiconductor layer 105, an i-type semiconductor layer 104, and a p-type or n-type semiconductor layer 103, and then a transparent electrode 102 such as of ITO and a grid (collector electrode) 101 on top. In this photovoltaic element the bottom photovoltaic element i-type semiconductor layer is constituted of microcrystalline silicon semiconductor.

[0026]

Figs. 3 through 5 show enlargements of the reflection increasing layer 109, the layer 108 having the first electric characteristics and the layer 107 having the second electric characteristics of Fig. 1.

[0027]

Fig. 3 is an example in which microcrystalline semiconductor layers 302 and 305 are grown almost just on a reflection increasing layer 301. The semiconductor layer having the first electric characteristics is the portion 305 below the straight line 303. The semiconductor layer having the second electric characteristics is the portion 302 above the straight line 303. Fig. 4 is an example in which an amorphous semiconductor layer is deposited on the reflection increasing layer 401 in several 100 A for example, and microcrystalline semiconductor layers 402 and 405 are grown thereon. The semiconductor layer having the first electric

characteristics is the portion 405 below the straight line 403. The semiconductor layer having the second electric characteristics is the portion 402 above the straight line 403. Fig. 5 is an example in which a microcrystalline semiconductor layer 504 is deposited on the reflection increasing layer 501 in several 100 A for example, and microcrystalline semiconductor layers 502 and 505 are grown thereon. The semiconductor layer having the first electric characteristics 505 is the portion below the straight line 503. The semiconductor layer having the second electric characteristics 502 is the portion above the straight line 503. In either example, a semiconductor junction is present within the microcrystal grains. The shape of the microcrystals having a semiconductor junction within the microcrystal grains is preferably a columnar shape when observed with a transmission electron microscope. One example of the preferred embodiments of the content of an additive for changing the electric characteristics of microcrystals having a semiconductor junction within microcrystal grains is such that the content is varied in the direction of thickness of the semiconductor layer having the first electric characteristics.

[0028]

Fig. 2 is an example of a deposited film forming apparatus for producing a photovoltaic element, which is an example of the semiconductor element of the present invention. This deposited film forming apparatus is constructed of a load chamber 201, a microcrystalline silicon i-type semiconductor layer deposition chamber 202, a silicon semiconductor layer (i-type semiconductor layer, p-type semiconductor layer, n-type

semiconductor layer) deposition RF chamber 203, a microcrystalline silicon germanium i-type semiconductor layer deposition chamber 204, and an unloading chamber 205. The loading chamber is equipped with a laser-annealing heater not shown in the drawing, and a window 222 for irradiating the semiconductor layer with a laser which is not shown in the drawing.

[0029]

Gate valves 206, 207, 208, and 209 separate each chamber so that the source gases do not mix. The microcrystalline silicon i-type semiconductor layer deposition chamber 202 is constructed of a heater 211 for substrate heating and a plasma CVD chamber 210. The RF chamber 203 is equipped with a heater 212 for n-type semiconductor layer deposition and a deposition chamber 215 for depositing the n-type semiconductor layer, a heater 213 for depositing the i-type semiconductor layer and a deposition chamber 216 for depositing the i-type semiconductor layer, and a heater 214 for depositing the p-type semiconductor layer and a deposition chamber 217 for depositing the p-type semiconductor layer. The microcrystalline silicon germanium i-type semiconductor layer deposition chamber 204 has a heater 218 and a plasma CVD chamber 219. A substrate is attached to a substrate holder 221, which is moved by a roller driven from the outside above a rail 220. For depositing the microcrystalline semiconductor, microwave plasma CVD method or VHF plasma CVD method are preferably used, but RF plasma CVD method can also be used.

[0030]

A photovoltaic element which is an example of the semiconductor element of the present invention, is formed as

described below.

[0031]

First, an SUS substrate 111 having a reflective layer 110 and a reflection increasing layer 109 formed thereon is set on the substrate holder 221, and then set on the rail 220 inside the loading chamber 201. The loading chamber 201 is exhausted to a vacuum degree under of several mTorr (1 Torr=133 Pa) or less. The gate valves 206 and 207 are opened, and the substrate holder is transferred to the n-type semiconductor layer deposition chamber 215 of the chamber 203. Each gate valve is closed and the n-type semiconductor layer 108 is deposited with desired source gases in a desired layer thickness. After exhausting sufficiently, the substrate holder is transferred to the loading chamber 201. The substrate is heated with a heater not shown in the drawing until the substrate temperature reaches 400°C, and after the substrate temperature has become constant, the n-type semiconductor layer 108 is crystallized with an XeCl laser not shown in the drawing. The internal pressure of the loading chamber during the laser irradiation is maintained at a degree of vacuum not higher than 10^{-3} Torr. The substrate holder is transferred to the microcrystalline silicon i-type semiconductor layer deposition chamber 202 and the gate valves 206 and 207 are closed. The substrate is heated with the heater 211 to a desired substrate temperature; a necessary amount of desired source gases are introduced; a desired degree of vacuum is attained; predetermined microwave energy or VHF energy is introduced into the deposition chamber 210; and a plasma is generated to deposit the microcrystalline silicon i-type semiconductor layer 107 in

a desired layer thickness on the n-type semiconductor layer 108. At this time, in order that the i-type semiconductor layer 107 is epitaxially grown on the n-type semiconductor layer 108, it is preferred that the i-type semiconductor layer 107 is deposited continuously after hydrogen plasma treatment of the n-type semiconductor layer 108 or that the substrate temperature during deposition of the i-type semiconductor layer 107 is made higher than the substrate temperature during deposition of the n-type semiconductor layer 108.

[0032]

Next, the chamber 202 is exhausted sufficiently; the gate valve 207 is opened; and the substrate holder 221 is transferred from the chamber 202 to the chamber 203. The substrate holder 221 is transferred to the p-type semiconductor layer deposition chamber 217 of the chamber 203, and the substrate is heated to a desired temperature with the heater 214. The deposition chamber 217 is supplied with source gases for p-type semiconductor layer deposition at a desired flow rate, and an RF energy is introduced into the deposition chamber 217 while maintaining a desired degree of vacuum in the deposition chamber 217. Then the p-type semiconductor layer 106 is deposited in a desired layer thickness. After depositing the p-type semiconductor layer 106, the deposition chamber 217 is exhausted sufficiently, and the substrate holder 227 is transferred to the n-type semiconductor layer deposition chamber 215 within the same chamber 203. An n-type semiconductor layer 105 is deposited on the p-type semiconductor layer 106 in the same way as the n-type semiconductor layer 108 mentioned previously. The deposition chamber 215 is exhausted sufficiently,

and the substrate holder 221 is transferred to the i-type semiconductor layer deposition chamber 216. The substrate is heated to a desired temperature with the heater 213. The deposition chamber 216 is supplied with source gases for i-type semiconductor layer deposition at a desired flow rate, and a desired RF energy is introduced while maintaining a desired pressure in the deposition chamber 216. Thereby the i-type semiconductor layer 104 is deposited in a desired film thickness on the n-type semiconductor layer 105. Next, the deposition chamber 216 is exhausted sufficiently; the substrate holder 221 is transferred from the deposition chamber 216 to the deposition chamber 217; and a p-type semiconductor layer 103 is deposited on the i-type semiconductor layer 104 in the same way as the p-type semiconductor layer 106 mentioned previously. After exhausting the deposition chamber 217 sufficiently in the same manner as mentioned previously, the gate valves 208 and 209 are opened, and the substrate holder 221 having set thereon the substrate with deposited semiconductor layers is transferred to the unloading chamber 205. All of the gate valves are closed, nitrogen gas is introduced into the unloading chamber 205; and the substrate is cooled to a desired temperature. Afterwards, the taking out valve of the unloading chamber 205 is opened to take out the substrate holder 221. Using a vaporizer for transparent electrode deposition (not shown), a transparent electrode 102 is deposited on the p-type semiconductor layer 103 in a desired layer thickness. Then, using the vaporizer (not shown) in the same way, a collector electrode 101 is deposited on the transparent electrode 102.

[0033]

Incidentally, when the microcrystalline i-type semiconductor layer 107 is formed by use of silicon germanium instead of silicon, the chamber 204 may be used instead of the chamber 202.

[0034]

Further, a semiconductor element having a semiconductor junction within microcrystal grains may also be formed in the following ways.

[0035]

(1) A crystalline semiconductor layer having first electric characteristics (a doped semiconductor layer), and then a microcrystalline semiconductor layer having second electric characteristics (a non-doped microcrystalline semiconductor layer or a microcrystalline semiconductor layer having a different electric characteristics from the first doped semiconductor layer) is deposited by changing the source gases under conditions such that microcrystals grow continuously, thus forming a semiconductor junction within the microcrystal grains.

[0036]

(2) A crystalline semiconductor layer having first electric characteristics is formed; a microcrystalline or amorphous semiconductor layer having second electric characteristics on the semiconductor layer; and the both semiconductor layers are annealed at a temperature below the melting points, thus forming a semiconductor junction within the microcrystal grains.

[0037]

(3) A microcrystalline semiconductor layer having first electric characteristics is formed; hydrogen plasma treatment

is applied onto the semiconductor layer to clean the surface of the microcrystalline semiconductor layer having the first electric characteristics; and then a microcrystalline semiconductor layer having second electric characteristics is epitaxially grown on the microcrystalline semiconductor layer having the first electric characteristics to form a semiconductor junction within the microcrystal grains.

[0038]

(4) An amorphous or crystalline semiconductor layer having first electric characteristics is formed; an amorphous or microcrystalline semiconductor layer having second electric characteristics is deposited on the semiconductor layer; and then recrystallization with an excimer laser (laser annealing) is carried out to form a semiconductor junction within the microcrystal grains.

[0039]

As the energy density of laser in recrystallization with an excimer laser, 200 mJ/cm^2 to 800 mJ/cm^2 is preferred. The total layer thickness of the first and the second semiconductor layers when effecting the laser annealing is preferably 100 A to 700 A. After recrystallization, epitaxially growing on the semiconductor layer with the second electric characteristics a semiconductor layer with the same electric characteristics makes it possible to increase the layer thickness of the semiconductor layer having the second electric characteristics. When performing the laser annealing, it is preferable to increase the environment temperature, specifically to 100-800°C. Particularly, when a supporting member (substrate) with low heat

resistance properties such as stainless thin film or glass is used, the environment temperature is preferably 100-600°C. Such lasers as ArF (wavelength: 193 nm), KrF (wavelength: 248 nm), XeCl (wavelength: 308 nm), or XeF (wavelength: 351 nm) are included as suitable ones for laser annealing. When annealing a silicon type semiconductor layer, XeCl (wavelength: 308 nm) is particularly preferable.

[0040]

(5) A crystalline semiconductor with first electric characteristics is formed and ion implanting an impurity (a dopant) in the semiconductor enables formation of a semiconductor junction within the same semiconductor.

[0041]

In this case, it is preferred that after ion implantation, thermal annealing is carried out within a range of 100 to 800°C.

[0042]

The present invention can be applied to formation of not only semiconductor junctions where one layer is not doped such as p/i or n/i junction, but also semiconductor junctions where the layers have opposite electric characteristics such as n/p junction, or semiconductor junctions where the layers have the same electric characteristics such as n/n or p/p but are different in dopant concentration from each other.

[0043]

The semiconductor layers adjacent to the semiconductor junction within the microcrystal grains (a semiconductor layer having first electric characteristics and a semiconductor layer having second electric characteristics) can be either amorphous

or crystalline during deposition if crystallization is carried out by a post-treatment. If no crystallization by a post-treatment is carried out, they need to be crystalline during deposition. When they are made crystalline during deposition, they are preferably microcrystalline semiconductors.

[0044]

The average crystal grain diameter of the microcrystal grains are preferably 100 A to 1000 A when obtained by calculation using the Scherrer's equation from the half-width of the X-ray diffraction (220) peak. If the average diameter is determined from the dark field image of a transmission electron microscope, it is preferably within 100 A to 10 μm. When the average crystal grain diameter of columnar microcrystals using a transmission electron microscope, it is preferred that a geometric mean of the long axis and the short axis thereof is within the above range.

[0045]

Further, the preferred proportion of amorphous phase contained in the microcrystalline semiconductor is such that when observed with the Raman spectrum, the ratio of amorphous phase related peaks to crystal phase related peaks is not more than 70%. If the average crystalline grain diameter is less than 100 A, more amorphous will exist on the crystal grain boundaries and photodeterioration is liable to be occurred. Also, if the crystal grain diameter is too small, there is a possibility that the mobility and life time of electrons and positive holes may be smaller to lower the characteristics as semiconductor. On the other hand, if the average crystal grain diameter calculated

using the Scherrer's equation is greater than 1000 A, there is a possibility that relaxation of the crystal grain boundaries may not progress sufficiently, defects such as dangling bonds may arise in the crystal grain boundaries, and the defects may act as recombination centers for electrons or positive holes, whereby the characteristics of the microcrystalline semiconductor may be lowered. As the shape of microcrystals, a shape which is long and thin (columnar) in the direction of movement of the charge is preferred. In addition, the proportion of hydrogen atoms or halogen atoms contained in the microcrystalline semiconductor layer of the present invention is preferably not more than 30%.

[0046]

The semiconductor layers used in the semiconductor element of the present invention include a doped layer such as a p-type semiconductor layer or n-type semiconductor layer, an i-type semiconductor layer, or the like.

[0047]

When the present invention is applied to a photovoltaic element, the doped layer is an important layer that influences the characteristics of the element, and the i-type semiconductor layer is also another important layer for carrier generation and transportation by light incidence.

[0048]

As the amorphous semiconductor materials, microcrystalline semiconductor materials and polycrystalline semiconductor materials that can preferably be applied to the semiconductor element of the present invention, there are included, for example,

a-Si:H, a-Si:HX, a-SiC:H, a-SiC:HX, a-SIGe:H, a-SiGeC:H, a-SiO:H, a-SiN:H, a-SiON:HX, a-SiOCN:HX, μc-Si:H, μc-SiC:H, μc-Si:HX, μc-SiC:HX, μc-SiGe:H, μc-SiO:H, μc-SiGeC:H, μc-SiN:H, μc-SiON:HX, μc-SiOCN:HX, poly-Si:H, poly-Si:HX, poly-SiC:H, poly-SiC:HX, poly-SiGe:H, poly-Si, Poly-SiC, and poly-SiGe can be used favorable.

[0049]

When these materials are applied to doped layers, it is preferable to add a p-type valency controller (Group III atoms of Periodic Table: B, Al, Ga, In, or Tl) or an n-type valency controller (Group V atoms of Periodic Table: P, As, Sb, or Bi) at a high concentration. The contents of Group III atoms in the p-type semiconductor layer and Group V atoms in the n-type semiconductor layer is preferably 0.1 to 50 atomic %.

[0050]

Further, the hydrogen atoms (H, D) and/or the halogen atoms (F, Cl, etc.) contained in the p-type semiconductor layer or the n-type semiconductor layer have a function of compensating for the dangling bonds of the p-type or the n-type semiconductor layer, thus improving the doping efficiency of the p-type or n-type semiconductor layer. The content of the hydrogen atoms and/or halogen atoms in the p-type or n-type semiconductor layer is preferably 0.1 to 40 atomic %. In particular, when the p-type or n-type semiconductor layer is crystalline, the content of hydrogen atoms and/or halogen atoms is preferably 0.1 to 8 atomic %.

[0051]

Further, for the semiconductor layers of the semiconductor element of the present invention, it is preferred that the content

of the hydrogen atoms (H, D) and/or the halogen atoms (F, Cl, etc.) is larger in the vicinity of each of the interfaces of p-type semiconductor layer/i-type semiconductor layer or n-type semiconductor layer/i-type semiconductor layer. Preferably, the content of the hydrogen atoms and/or halogen atoms in the vicinity of the interfaces is preferably within a range of 1.1 to 2 times the content of the bulk area in the case of the p-type semiconductor layer or the n-type semiconductor layer, and is preferably within a range of 1.1 to 2 times the content of the bulk area in the case of the i-type semiconductor layer. Such larger contents of hydrogen atoms or halogen atoms in the vicinity of the interfaces (p-type semiconductor layer/i-type semiconductor layer, n-type semiconductor layer/i-type semiconductor layer) can reduce defect states and mechanical distortions in the vicinity of the interfaces, thereby improving the characteristics of the semiconductor element of the present invention.

[0052]

When a multiple-element (alloy) semiconductor layer such as SiC, SiGe, etc., it is preferable that the content of hydrogen atoms and/or halogen atoms is changed in response to the change in content of silicon atoms. In the semiconductor layer, depending on the bandgap, the content of hydrogen atoms and/or halogen atoms is smaller at a portion of narrow bandgap. Incidentally, it is preferred that the content of the hydrogen atoms and/or halogen atoms at a portion where the content of silicon atoms is the minimum is 1 to 10 atomic %, and is 0.3 to 0.8 times the content at a portion where the content of hydrogen atoms and/or

halogen atoms is the maximum.

[0053]

Although the details of the mechanism are not clear, it is considered that when a alloy semiconductor containing silicon atoms and germanium atoms is deposited, a difference arises in the electromagnetic wave energies acquired by each of the atoms due to the differences in ionization rates of the silicon atoms and germanium atoms, with the result that even if the content of the hydrogen and/or halogen in the alloy semiconductor is small, the relaxation proceeds sufficiently to provide a high quality alloy semiconductor.

[0054]

The preferred electric characteristics for the p-type semiconductor layer and the n-type semiconductor layer when applying the semiconductor element of the present invention to a photovoltaic element is such that the activation energy is not more than 0.2 eV, optimally not more than 0.1 eV. The resistivity is preferably not more than 100 Ωcm, optimally not more than 1 Ωcm. The layer thickness of the p-type semiconductor layer and the n-type semiconductor layer is preferably 1 to 50 nm, optimally 3 to 10 nm.

[0055]

As the p-type semiconductor layer or the n-type semiconductor layer on the light incidence side, a crystalline semiconductor layer with less absorption of light or an amorphous semiconductor layer with a large bandgap is suitable.

[0056]

As the i-type semiconductor layer in the semiconductor element

of the present invention, a semiconductor layer that is slightly of the p-type or n-type (i.e., substantially i-type semiconductor layer) can be used (whether it becomes the p-type or n-type depends on the distribution of characteristic defects such as tail state).

[0057]

As the i-type semiconductor layer when the semiconductor element of the present invention is applied to a photovoltaic element, there can suitably be used, in addition to semiconductors with a uniform bandgap, those semiconductor which contain silicon atoms and germanium atoms such that the bandgap changes smoothly in the direction of layer thickness of the i-type semiconductor layer, and that the minimum of the bandgap is offset from the central position of the i-type semiconductor layer toward the interface between the p-type semiconductor layer and the i-type semiconductor layer. Further, a semiconductor layer doped with both a valency controller to be a donor and a valency controller to be an acceptor is also suitable as the i-type semiconductor layer.

[0058]

Further, it is preferred that the bandgap of the i-type semiconductor layer is so designed that it becomes greater toward each of the interfaces of p-type semiconductor layer/i-type semiconductor layer and n-type semiconductor/i-type semiconductor layer. Such design makes it possible to increase the photovoltage and photocurrent of the photovoltaic element and to prevent photodeterioration in long-term use, or the like.

[0059]

The preferred layer thickness of the i-type semiconductor

layer in the case of a photovoltaic element depends largely on the structure of the element (for example single cell, tandem cell, or triple cell) and on the bandgap of the i-type semiconductor layer, but 0.7 to 30.0 μm is a suitable thickness.

[0060]

Next, as the preferred methods for deposition of semiconductor layers of the semiconductor element of the present invention, there are included RF plasma CVD, VHF plasma CVD, and microwave plasma CVD. The preferred range for the frequency of RF and VHF is 1 MHz to 300 MHz. For RF, a frequency in the vicinity of 13.56 MHz is optimal, and for VHF a frequency in the vicinity of 105 MHz is optimal. For the microwave, 0.5 GHz to 10 GHz is a preferred frequency range.

[0061]

In particular, when depositing microcrystalline silicon, since the deposition rate depends on the electromagnetic wave used and becomes larger with increasing frequency in a given input energy, using high frequency electromagnetic waves is suitable.

[0062]

As the source gases suitable for deposition of the semiconductor layers of the semiconductor element of the present invention, there can be included a gas comprised of a gasifiable compound containing silicon atoms, a gas comprised of a gasifiable compound containing germanium atoms, a gas comprised of a gasifiable compound containing carbon atoms, or a mixture gas thereof.

[0063]

As the compounds which contains silicon atoms and are gasifiable, there are included, for example, SiH_4, Si_2H_6, Si_3H_8, SiF_4, $SiHF_3$, SiH_2F_2, SiH_3F, SiH_3Cl, SiH_2Cl_2, $SiHCl_3$, $SiCl_4$, SiD_4, $SiHD_3$, SiH_2D_2, SiH_3D, SiD_3F, SiD_2F_2, $SiHD_3$, $Si_2H_3D_2$, etc.

[0064]

As the compounds which contains germanium atoms and are gasifiable, there are included, for example, germanium compounds such as GeH_4, GeF_4, $GeHF_3$, GeH_2F_2, GeH_3F, $GeHCl_3$, GeH_2Cl_2, GeH_3Cl, $GeHD_3$, GeH_2D_2, GeH_3D, GeD_4, Ge_2H_6, Ge_2D_6, etc.

[0065]

As the compounds which contains carbon atoms and are gasifiable, there are included, for example, compounds represented by C_nH_{2n+2} (n is an integer) such as CH_4, etc., compounds represented by C_nH_{2n} (n is an integer) such as C_2H_2, etc., and CD_4, C_6H_6, CO_2, CO, or the like.

[0066]

Further, the source gases may contain a gas that contains nitrogen atoms or a gas that contains oxygen atoms.

[0067]

The gases containing nitrogen atoms include N_2, NH_3, ND_3, NO, NO_2, N_2O, etc.

[0068]

The gases containing oxygen atoms include gases as O_2, CO, CO_2, NO, NO_2, N_2O, CH_3CH_2OH, CH_3OH, etc.

[0069]

Further, the above gasifiable compounds may be suitably diluted with such gases as H_2, He, Ne, Ar, Xe, or Kr to be introduced into the deposition chamber.

[0070]

In particular, when depositing a microcrystalline semiconductor layer of the present invention, it is preferred that these source gases are diluted with hydrogen gas or helium gas in order to form a good microcrystalline semiconductor. The dilution rate with hydrogen gas is preferably 10 or more fold. The especially preferred range of dilution rate is from 10 to 100 fold. If the dilution rate is too small, formation of microcrystals becomes difficult and amorphous phase is liable to be formed. On the other hand, if the dilution rate is too large, the microcrystal deposition rate is too small and problems in practical use arise.

[0071]

In particular, when depositing microcrystalline semiconductor or a semiconductor layer with less light absorption or with a large bandgap such as a-SiC:H or the like, it is preferable to dilute the source gas 2 to 100 fold with hydrogen gas, etc. and to make the input RF power, VHF power, or microwave power relatively high.

[0072]

When depositing a p-type semiconductor layer or an n-type semiconductor layer, it is preferable to add a compound that contains a valency controller (Group III or Group V atoms of Periodic Table) to the source gases in order to effect valency control.

[0073]

As the compounds for introducing Group III atoms, there can effectively be used boron hydrides such as B_2H_6, B_4H_{10}, B_5H_9,

B_5H_{11}, B_6H_{10}, B_6H_{12}, B_6H_{14}, etc. or boron halides such as BF_3, BCl_3, etc. for boron atom introduction. In addition, such compounds as $AlCl_3$, $GaCl_3$, $InCl_3$, or $TlCl_3$ can be included as compounds for introducing Group III atoms other than boron. Of these compounds B_2H_6 and BF_3 are especially suitable.

As the compounds for introducing Group V atoms, there can effectively be used phosphorous hydrides such as PH_3, P_2H_4, etc. and phosphorous halides such as PH_4I, PF_3, PF_5, PCl_3, PCl_5, PBr_3, PBr_5, PI_3, etc. for phosphorous atom introduction. In addition, such compounds as AsH_3, AsF_3, $AsCl_3$, $AsBr_3$, AsF_5, SbH_3, SbF_3, SbF_5, $SbCl_3$, $SbCl_5$, BiH_3, $BiCl_3$, and $BiBr_3$ can be included as compounds for introducing Group V atoms other than phosphorous. Of these compounds PH_3 and PF_3 are especially suitable.

[0074]

When depositing a semiconductor layer with the RF plasma CVD method mentioned previously, the preferred deposition conditions are such that the substrate temperature in the deposition chamber is 100 to 350°C; the internal pressure is 0.1 to 10 Torr, the RF power is 0.01 to 5.0 W/cm^2, and the deposition rate is 0.1 to 30 A/sec. Further, when depositing a semiconductor layer with the RF plasma CVD method, the capacitive coupled RF plasma CVD method is suitably used.

[0075]

When depositing a semiconductor layer with the microwave plasma CVD method, the preferred deposition conditions are such that the substrate temperature in the deposition chamber is 100 to 400°C, the internal pressure is 0.5 to 30 mTorr, and the microwave power is 0.01 to 1.0 W/cm^3. As the microwave plasma CVD apparatus

used when depositing a semiconductor layer by microwave plasma CVD method, a method is suitable in which the microwaves are introduced by a waveguide through a dielectric window (such as of aluminum ceramics) into the deposition chamber.

[0076]

The substrate temperature for depositing a microcrystalline semiconductor layer suited to the present invention is 100 to 500°C. It is desirable that when increasing the deposition rate is desired, the substrate is kept at a relatively high temperature. As a suitable range for degree of vacuum in the chamber during deposition of the microcrystalline semiconductor layer of the present invention, the range of 1 mTorr - 1 Torr is included. Especially when depositing the microcrystalline semiconductor layer by the microwave plasma CVD method, 1 mTorr - 10 mTorr is preferable as the degree of vacuum.

[0077]

As a suitable range for input power for the chamber when depositing the microcrystalline semiconductor layer of the present invention, 0.01 - 10 W/cm^3 is included. When it is defined by the relationship of source gas flow rate and input power, the power limited region is suitable in which the deposition rate depends on the input power.

[0078]

Further, the distance between the substrate and the electrodes for power input is an important factor in the deposition of the microcrystalline semiconductor layer of the present invention. In order to obtain a microcrystalline layer suited to the present invention it is preferred to set the distance to be 10 mm - 50

mm.

[0079]

The i-type semiconductor layer containing silicon atoms or germanium atoms formed by the above described deposited film formation method is such that there are less tail states on the valence band side even when the deposition rate is over 5 nm/sec, and that the tail states have an inclination of not more than 60 meV, and that the density of dangling bonds determined by the electron spin resonance (esr) is not more than $10^{17}/cm^3$.

[0080]

The present invention is explained in detail below based on Examples. Of course, it is to be understood that the present invention is not limited to the following examples.

[0081]

[examples]

(Example 1)

In this example a photovoltaic element was produced using the deposited film forming apparatus shown in Fig. 2. The deposition conditions of each of the semiconductor layers are shown in Table 1. The formation of the members such as electrodes in all the examples including this example and comparative examples was made following a conventional method. The microcrystalline semiconductor having a semiconductor junction within the same microcrystalline semiconductor of the present invention was used between the n-type semiconductor layer n1 and an i-type semiconductor layer i1 of the bottom photovoltaic element. After deposition of the n-type semiconductor layer n1, the n-type semiconductor layer n1 was irradiated with an excimer laser under

the conditions shown in Table 2 in the loading chamber to crystalize the n-type semiconductor layer n1. Afterwards, the i-type semiconductor layer i1 was successively deposited on the n-type semiconductor layer n1 by the VHF plasma CVD method.

[0082]

(Comparative Example 1)

A photovoltaic element for comparison with Example 1 was produced in a similar manner to that of Example 1 with the exception that the n-type semiconductor layer n1 was not treated with an excimer laser.

[0083]

(Comparison of Example 1 with Comparative Example 1)

The characteristics of the photovoltaic element thus formed were measured and evaluated using WXS-130S-20T (trade name; mfd. by WACOM CO.) as a light source. The spectrum of the light source was AM 1.5 and the light intensity was 1 sun. The results are shown in Table 3 in terms of relative values when the results of Comparative Example 1 are expressed as 1. The photovoltaic element of Example 1 comprising microcrystalline semiconductor with a semiconductor junction within the same microcrystalline semiconductor of the present invention showed excellent photovoltaic characteristics compared to the Comparative Example 1 element. Further, as compared with the Comparative Example 1 element, the photovoltaic element of Example 1 had a lower series resistance and a larger shunt resistance.

[0084]

Then, 100 photovoltaic elements each were produced under the same conditions as Example 1 and Comparative Example 1.

These photovoltaic elements were allowed to stand for 2000 hours in an atmosphere containing acetic acid at 85°C temperature and 85% humidity. Afterwards, the photovoltaic characteristics were measured. Compared to the elements of Comparative Example 1, the characteristics of the 100 photovoltaic elements of Example 1 showed an extremely small variance. In other words, the photovoltaic elements of the present invention had an extremely high resistance to environment (durability).

[0085]

When a cross section of each of these photovoltaic elements was observed with a transmission electron microscope, it was confirmed for the photovoltaic elements of Example 1 that the region thought to be the boundary between the n-type semiconductor layer and the i-type semiconductor layer was constituted of microcrystal grains with a length in the layer thickness direction of 2000 - 4000 A. Further, it was confirmed through secondary ion mass spectroscopy that the impurities (dopant) were localized on the substrate side of the microcrystal grains.

[0086]

(Example 2)

A photovoltaic element was produced under the deposited film formation conditions shown in Table 4 using the deposited film forming apparatus of Fig. 2 in the same manner as in Example 1. The n-type semiconductor layer n1 was irradiated with an excimer laser under the conditions shown in Table 5 to crystallize it in a similar manner to that of Example 1. A bottom i-type semiconductor layer i1 was deposited thereon by the so-called HRCVD method in which hydrogen gas was activated with microwave

plasma and reacted with SiF_4 to deposit a semiconductor layer.

[0087]

(Comparative Example 2)

A photovoltaic element was produced in a similar manner to that of Example 2 with the exception that the n-type semiconductor layer n1 was not treated with a laser.

[0088]

(Comparison of Example 2 and Comparative Example 2)

The photovoltaic element characteristics of these photovoltaic elements were measured in a similar manner to that of Example 1 and Comparative Example 1. The results are shown in Table 6 in terms of relative values when the results of Comparative Example 2 are expressed as 1. The photovoltaic element of Example 2 showed superior photovoltaic characteristics in comparison to the Comparative Example 2 element.

[0089]

Further, a cross section of each of these photovoltaic elements was observed with an electron microscope and the amount of impurities was measured by secondary ion mass spectroscopy. As a result, it was confirmed for the photovoltaic element of Example 2 that a portion of each of the n-type semiconductor layer and the i-type semiconductor layer were formed within the same microcrystal grains. The shape of the microcrystal grains was columnar, the length in the layer thickness direction was 3000 A, and the length in the direction perpendicular to the layer thickness direction was 300 A.

[0090]

(Example 3)

A photovoltaic element was produced in a similar manner to that of Example 1 with the exception that in place of the method of Example 1 in which the i-type semiconductor layer i1 was stacked on the n-type semiconductor layer n1 crystallized by laser, a method was used in which after depositing the n-type semiconductor layer n1, a hydrogen plasma treatment shown in Table 7 was performed in the i-type semiconductor layer deposition chamber 202, and a source gas for formation of an i-type semiconductor layer was added without discontinuing the discharge to deposit the i-type semiconductor layer i1.

[0091]

(Comparison of Example 3 and Comparative Example 1)

The photovoltaic characteristics of the photovoltaic element of Example 3 were evaluated in a similar manner to that of Example 1. The results are shown in Table 8 in terms of relative values when the results of Comparative Example 1 are expressed as 1.

[0092]

As is clear from Table 8, the photovoltaic element of Example 3 showed superior photovoltaic characteristics.

[0093]

(Example 4)

Using the deposited film forming apparatus shown in Fig. 2, a photovoltaic element was formed under the deposited film formation conditions shown in Table 9. After depositing a microcrystalline i-type semiconductor layer (i0 layer), phosphorous atoms were implanted into the i0 layer under the conditions shown in Table 10 with an ion implantation apparatus not shown, followed by annealing to activate the phosphorous

atoms.

[0094]

(Comparison of Example 4 and Comparative Example 1)

The photovoltaic characteristics of the photovoltaic element of Example 4 were evaluated in a similar manner to that of Example 1. The results are shown in Table 11 in terms of relative values when the results of Comparative Example 1 are expressed as 1.

[0095]

As is clear from Table 11, the photovoltaic element of Example 4 showed superior photovoltaic characteristics.

[0096]

When a cross section of the photovoltaic element of Example 4 was observed with an electron microscope, it was confirmed for the i0 layer that uniform microcrystal grains were formed extending over the whole in the layer thickness direction in a layer thickness of 3000 A. It was further confirmed through secondary ion mass spectroscopy that the implanted phosphorous atoms were distributed only on the substrate side, namely that a semiconductor junction was formed within a single microcrystal grain.

[0097]

(Example 5)

Using the deposited film forming apparatus shown in Fig. 2, a photovoltaic element was formed under the deposited film formation conditions shown in Table 12. The microcrystalline semiconductor having a semiconductor junction within the same microcrystal grain was used between the n-type and the i-type semiconductor layers n1 and i1 of the bottom photovoltaic element.

After deposition of the n-type semiconductor layer n1, the n-type semiconductor layer n1 was irradiated with an excimer laser under the conditions shown in Table 2 in the loading chamber to crystallize the n-type semiconductor layer n1. Afterwards, an i-type semiconductor layer i1 was successively deposited on the n-type semiconductor layer n0 with the VHF plasma CVD method.

[0098]

(Comparative Example 3)

A photovoltaic element for comparison with Example 5 was produced in a similar manner to that of Example 5 with the exception that the n-type semiconductor layer was not treated with an excimer laser.

[0099]

(Comparison of Example 5 and Comparative Example 3)

The photovoltaic element characteristics of these photovoltaic elements were measured in a similar manner to that of Example 1 and Comparative Example 1. These results are shown in Table 13 in terms of relative values when the results of Comparative Example 3 are expressed as 1. The photovoltaic element of Example 5 showed photovoltaic characteristics superior to the element of Comparative Example 3. Also, the photovoltaic element of the present invention had lower series resistance and larger shunt resistance in comparison with the element of Comparative Example 3.

[0100]

One hundred photovoltaic elements each were then produced under the same conditions as Example 5 and Comparative Example 3. These photovoltaic elements were then left for 2000 hours

in an atmosphere of 85°C temperature and 85% humidity. Afterwards their photovoltaic characteristics were measured. The 100 photovoltaic elements of Example 5 had an extremely small variance of the characteristics as compared with the elements of Comparative Example 3. In other words, the photovoltaic elements of the present invention have extremely high resistance to environment (durability).

[0101]

When a cross section of each of these photovoltaic elements was observed with a transmission electron microscope, it was confirmed for the photovoltaic elements of Example 5 that the region thought to be the boundary between the n-type semiconductor layer and the i-type semiconductor layer was constituted of microcrystal grains 2000 - 5000 A long in the film thickness direction. It was also confirmed through secondary ion mass spectroscopy that the impurities (dopant) were localized on the substrate side of these microcrystal grains.

[0102]

(Example 6)

A photovoltaic element was produced in a similar manner to that of Example 1 with the exception that after depositing the p-type semiconductor layer, the p-type semiconductor layer was irradiated with an excimer laser under the same conditions of laser irradiation as the crystallization of the n-type semiconductor layer, i.e., the conditions shown in Table 2. Through this irradiation a microcrystalline layer was formed having a semiconductor junction within the microcrystal grain, further between the i-type semiconductor layer and the p-type

semiconductor layer.

[0103]

(Comparison of Example 6 with Example 1 and Comparative Example 1)

The photovoltaic element of Example 6 was evaluated in a similar manner to that of Example 1. These results are shown in Table 14 in terms of relative values when the results of Comparative Example 1 are expressed as 1. The photovoltaic element of Example 6 showed excellent characteristics in comparison with the element of Comparative Example 1 and the element of Example 1.

[0104]

A transmission electron microscope and a secondary ion mass spectrometer were used to confirm whether or not a semiconductor junction was formed within the same microcrystal grain in the photovoltaic element of this example. As a result, it was confirmed that the element of this example had the n-type semiconductor layer and the i-type semiconductor layer within the same microcrystal grains and had the i-type semiconductor layer and the p-type semiconductor layer within the same microcrystal grains.

[0105]

From the above, it was confirmed that the photovoltaic element having the n-type semiconductor layer and the i-type semiconductor layer within the same microcrystal grains and having the i-type semiconductor layer and the p-type semiconductor layer within the same microcrystal grains has the best characteristics.

[0106]

One hundred photovoltaic elements each of Example 6 and

Comparative Example 1 were then produced, and left for 3000 hours in an atmosphere of a nitrogen oxide at 85°C temperature and 95% humidity while irradiating them with light of AM 1.5 and 100 mW/cm^2. Afterwards their photovoltaic characteristics were measured. The photovoltaic elements of Example 6 had less change in characteristics than the elements of Comparative Example 1.

[0107]

Further, the current values when a 2V reverse bias was applied to the photovoltaic elements of Example 6 and the elements of Comparative Example 1 were compared. The results showed that the current values of the photovoltaic elements of Example 6 were approximately one order lower than those for the elements of Comparative Example 1.

[0108]

[Table 1]

Table 1

		Gas				Power Density (W/cm^3)		Vacuum Degree (mTorr)	Deposition Rate (Å/s)	Substrate Temperature (°C)	Layer Thickness (Å)
		SiH_4	H_2	PH_3 (2% H_2)	BF_3 (2% H_2)	RF	VHF				
Bottom	n1	2	48	0.5		0.0382		1300	1	225	200
	i1	25	750				0.12	300	1	250	15000
	p1	0.025	35		1	1.15		2000	1	165	50
Top	n2	2	48	0.5		0.0382		1300	1	225	100
	i2	2	48			0.0382		1150	1	200	3000
	p2	0.025	35		1	1.15		2000	1	165	50

[0109]

[Table 2]

Table 2

Excimer Laser	Wave Length	Output	Vacuum Degree
	nm	mJ/cm^2	Torr
XeCl	308	500	1E-05

[0110]

[Table 3]

Table 3

	Open Circuit Voltage	Short Circuit Current	Fill Factor	Conversion Efficiency
Comparative Example 1	1	1	1	1
Example 1	1.02	1	1.03	1.05

[0111]

[Table 4]

Table 4

		Gas					Power Density (W/cm^3)			Vacuum Degree (mTorr)	Deposition Rate (Å/s)	Substrate Temperature (°C)	Layer Thickness (Å)
		SiH_4	SiF_4	H_2	PH_3 (2% H_2)	BF_3 (2% H_2)	RF	VHF	MW				
Bottom	n1	2		48	0.5		0.0382			1300	1	225	200
	i1		100	300					0.6	250	20	250	20000
	p1	0.025		35		1	1.15			2000	1	165	50
Top	n2	2		48	0.5		0.0382			1300	1	225	100
	i2	2		48			0.0382			1150	1	200	3500
	p2	0.025		35		1	1.15			2000	1	165	50

[0112]

[Table 5]

Table 5

Excimer Laser	Wave Length	Output	Vacuum Degree
	nm	mJ/cm^2	Torr
XeCl	308	600	1E-05

[0113]

[Table 6]

Table 6

	Open Circuit Voltage	Short Circuit Current	Fill Factor	Conversion Efficiency
Comparative Example 2	1	1	1	1
Example 2	1.02	1	1.02	1.04

[0114]

[Table 7]

Table 7

Hydrogen Flow Rate (sccm)	Current Density (W/cm^3)	Vacuum Degree (Torr)	Substrate Temperature (°C)
100	0.1	0.5	300

[0115]

[Table 8]

Table 8

	Open Circuit Voltage	Short Circuit Current	Fill Factor	Conversion Efficiency
Comparative Example 1	1	1	1	1
Example 3	1.02	1.01	1.02	1.05

[0116]

[Table 9]

Table 9

		Gas				Power Density (W/cm^3)		Vacuum Degree (mTorr)	Deposition Rate (Å/s)	Substrate Temperature (°C)	Layer Thickness (Å)
		SiH_4	H_2	PH_3 (2% H_2)	BF_3 (2% H_2)	RF	VHF				
Bottom	i0	25	750				0.12	300	1	250	3000
	i1	25	750				0.12	300	1	250	14000
	p1	0.025	35		1	1.15		2000	1	165	50
Top	n2	2	48	0.5		0.0382		1300	1	225	100
	i2	2	48			0.0382		1150	1	200	3000
	p2	0.025	35		1	1.15		2000	1	165	50

[0117]

[Table 10]

Table 10

Addition Amount ($1/cm^3$)	Vacuum Degree (Torr)	Substrate Temperature (°C)	Annealing Temperature (°C)
1E+20	1E-07	300	600

[0118]

[Table 11]

Table 11

	Open Circuit Voltage	Short Circuit Current	Fill Factor	Conversion Efficiency
Comparative Example 1	1	1	1	1
Example 3	1.02	1.01	1.03	1.06

[0119]

[Table 12]

Table 12

		Gas					Power Density (W/cm^3)		Vacuum Degree (mTorr)	Deposition Rate (Å/s)	Substrate Temperature (°C)	Layer Thickness (Å)
		SiH_4	GeH_4	H_2	PH_3 (2% H_2)	BF_3 (2% H_2)	RF	VHF				
Bottom	n1	1	1	48	0.5		0.0382		1300	1	225	200
	i1	12	12	750				0.12	300	1	250	10000
	p1	0.025		35		1	1.15		2000	1	165	50
Top	n2	2		48	0.5		0.0382		1300	1	225	100
	i2	2		48			0.0382		1150	1	200	3500
	p2	0.025		35		1	1.15		2000	1	165	50

[0120]

[Table 13]

Table 13

	Open Circuit Voltage	Short Circuit Current	Fill Factor	Conversion Efficiency
Comparative Example 3	1	1	1	1
Example 5	1.01	1.01	1.01	1.03

[0121]

[Table 14]

Table 14

	Open Circuit Voltage	Short Circuit Current	Fill Factor	Conversion Efficiency
Comparative Example 1	1	1	1	1
Example 1	1.02	1	1.03	1.05
Example 6	1.03	1.01	1.04	1.08

[0122]

[Effect of the Invention]

The defect states in the vicinity of the interfaces can be greatly reduced by forming semiconductor junctions such as p/i or n/i within the same microcrystal grains. As a result it is possible to prevent a decline in the open circuit voltage (Voc), short circuit current (Jsc), and fill factor (FF) of the photovoltaic element. Further, it is possible to prevent an increase in the series resistance and a decline in the shunt resistance of the photovoltaic element. As a result the photoelectric conversion efficiency of the photovoltaic device is improved.

[0123]

The heat resistant properties of the semiconductor element also improves due to the formation of a semiconductor junction within the microcrystal grains.

[0124]

In addition, it is possible to prevent degradation in characteristics caused by air or an encapsulant by forming a semiconductor junction within the microcrystal grains.

[0125]

Further, a depletion layer of a semiconductor junction spreads further than in semiconductor elements having conventional semiconductor junctions, by forming a semiconductor junction within microcrystal grains. As a result the rectifying characteristics are better than in conventional semiconductor junctions and the dark current is kept lower when a reverse bias is applied.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Fig. 1] is a schematic sectional view showing an example of the layer structure of a photovoltaic element, which is an example of the semiconductor element of the present invention.

[Fig. 2] is a schematic view showing an example of a deposited film forming apparatus for producing a photovoltaic element, which is an example of the semiconductor element of the present invention.

[Fig. 3] is a schematic sectional view showing an example in which a microcrystalline semiconductor layer is grown almost just above a reflection increasing layer.

[Fig. 4] is a schematic sectional view showing an example in which an amorphous layer is deposited on a reflection increasing layer, and a microcrystalline semiconductor layer is grown thereon.

[Fig. 5] is a schematic sectional view showing an example in which a microcrystalline semiconductor layer is deposited on a reflection increasing layer, and another microcrystalline semiconductor layer is grown thereon.

[Explanation of Reference Signs]

101 Grid (Collecting electrode)

102 Transparent electrode

103 P-type or n-type semiconductor layer

104 I-type semiconductor layer

105 N-type or p-type semiconductor layer

106 P-type or n-type semiconductor layer

107 I-type semiconductor layer

108 N-type or p-type semiconductor layer

109 Reflection increasing layer

110 Reflection layer

111 Substrate

112 Bottom photovoltaic element

113 Top photovoltaic element

210 Load chamber

202 Microcrystalline silicon i-type semiconductor layer deposition chamber

203 Silicon deposition RF chamber

204 Microcrystalline silicon germanium i-type semiconductor layer deposition chamber

205 Unloading chamber

206, 207, 208, 209 Gate valve

210, 219 Plasma CVD chamber

211, 218 Heater

212 Heater for n-type semiconductor layer deposition

213 Heater for i-type semiconductor layer deposition

214 Heater for p-type semiconductor layer deposition

215 Deposition chamber for n-type semiconductor layer deposition

216 Deposition chamber for i-type semiconductor layer deposition

217 Deposition chamber for p-type semiconductor layer deposition

220 Rail

221 Substrate holder

222 Window for irradiation with laser

301, 401, 501 Reflection increasing layer

302, 402, 502 Portion of layer with second electric characteristics of microcrystalline semiconductor layer

303, 403, 503 Straight line showing boundary at which electric characteristics change

305, 405, 505 Portion of layer with second electric characteristics of microcrystalline semiconductor layer

504 Microcrystalline semiconductor layer

[NAME OF DOCUMENT] ABSTRACT

[ABSTRACT]

[OBJECT] To improve discontinuity of a semiconductor junction to thereby improve the characteristics, durability, and heat resisting properties of a semiconductor element.

[MEANS FOR ATTAINING OBJECT]

In a semiconductor element comprising microcrystalline semiconductor, a semiconductor junction is provided within a microcrystal grain.

[ELECTED FIGURE] FIGURE 3